Remarks

Claims 60-89 are pending in the present application, with claims 64 and 76-79 having been withdrawn as being directed to an unelected species. Claim 60 has been amended herein and remains generic. Claim 75 has also been amended to be consistent with the amendment of claim 60. In view of the following remarks, allowance of claims 60-89 is respectfully requested.

Each of the pending claims has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nowak et al. (U.S. Patent No. 6,100,153) in view of Yu et al. (U.S. Patent No. 6,784,101). Applicant respectfully traverses this rejection.

Claim 60, as currently amended, specifically recites "forming a resistor body of a first conductivity type in a portion of the silicon layer; forming a dielectric layer overlying the body region, the dielectric layer comprising a material with a relative permittivity greater than about 8; forming a top electrode on the dielectric layer, the top electrode comprising a conductive material; and forming a pair of doped regions of the first conductivity type oppositely adjacent the body region." It is respectfully submitted that the references of record do not teach or suggest the limitations of claim 60.

In particular, Nowak et al. specifically teaches that the gate 58 is not doped. Fig. 3. In fact, Nowak et al. teaches that this is an important feature of the invention.

> Accordingly, a buried resistor is provided that utilizes a block mask which covers only the intrinsic polysilicon region. Thus, the n-type source/drain doping will be applied to the resistor terminal region (or contact region) but not in the intrinsic polysilicon region. This reduces the parasitic diffusion-to-polysilicon capacitance, improves the reliability performance, ensures the good ohmic contact, and keeps the spreading resistance low

Col. 2, lines 15-22. By using an intrinsic, i.e., undoped, polysilicon gate, the resistance in the gate is kept very large, and the current flowing through the undoped poly-silicon gate between the input (78 of Fig. 4) and output (80 of Fig. 4) is negligible compared with the main current flowing through the

body of the resistor. Any current flowing through the SiO_2 gate dielectric is therefore small as well. There is no special motivation for one skilled in the art to combine Nowak et al. with Yu et al. to suppress the already small leakage current.

The present invention, however, requires a top electrode formed from a conductive material. The specification and dependent claims provide several examples of conductive materials to use for the gate electrode. See e.g., Pars. [0029]-[0030]; claims 75-79. By using conductive materials such as doped semiconductor, metal, metallic nitride, metal silicide and metal oxide, the gate electrode overlying the resistor body can be formed together with the gate electrode in transistors formed elsewhere on the same chip, allowing easy integration of resistor and transistor without special steps.

Further, as admitted in the Office Action, Nowak does not teach that the dielectric layer comprise a material with a relative permittivity greater than about 8. Applicant submits that Yu does not teach anything to suggest modification of the Nowak reference. In combining the two prior art references, the Office Action states that it would have been obvious to one of ordinary skill in the art to form the gate of Nowak by the method of Yu to form a high k dielectric layer because it allows for greater capacitance and device speed with less gate-to-channel leakage current. This rationale, however, directly contradicts the stated goal of Nowak, which is to reduce the parasitic diffusion-to-polysilicon capacitance. Nowak, col. 2, lines 18-20. Since Nowak and Yu teach opposite goals (i.e., Nowak teaches to reduce capacitance and Yu teaches to increase capacitance), combination of these references is improper.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the address below.

No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

Ira S. Matsil
Attorney for Applicants
Reg. No. 35,272

Slater & Matsil, L.L.P.
17950 Preston Rd.
Suite 1000
Dallas, TX 75252-5793
972-732-1001 - Tel
972-732-9218 - Fax